Note to Accompany QS-1 Cards; January 1988

The QS-1 is not on "general release" yet.

I have begun the task of writing the documentation for the QS-1 board. There is sufficient information already in the document with which you have already been issued to allow the board to be constructed, and the purpose of the various jumper links not mentioned explicitly can be deduced from a study of the circuit diagram.

However before the card can be supplied to a wider audience I must provide at least the following additional information:

1. Discussion of the purpose of all jumper links and pin assemblies which have not been discussed so far.

2. Discussion of software matters and card select control bits; example of software initialisation table for Z8Ø-DART/SIO chip.

As the absence of neither of the above prevents the card being constructed, I have thought it sensible to send you your QS-1 card(s) now so that you can get on with the job whilst you are waiting for me.

David M Parkins
Greenbank Electronics

18-11-87.

Circuit Description DRAFT ONLY, REQUIRES MORE WORK

The circuit description is given with reference to the various sheets of the diagrams

Sheet 1 Block Diagram

This gives an overall view of the circuit and acts as a "map" saying on what sheet the detailed circuit will be found. The ideal would be to have the entire circuit on one sheet of paper, but this would be either an excessively large sheet of paper or the writing would be excessively small. The block diagram is a compromise; it is on one sheet but in consequence cannot include all the detailed connections etc.

Sheet 2 Input Buffers, Decode Logic

To the top and left of this diagram are the various buffer chips which provide the interface to the edge connector signals (and hence to the back board). The principle followed is that every signal used on this board both in and out in and out is to be buffered. This does result in the provision of an extra 4 or 5 integrated circuits but gives several benefits:

1. Loading on the back board. The load on the back board does not exceed 1 input line per signal per board. This is of most significance when 74LS and the like buffering is used in a system. Each card for example could drive a dozen other cards in the system plus the load presented by any bus termination components. This is tolerable, but if input buffers were not used on each card and (to exaggerate) each input signal line on a typical card went to 4 or 5 inputs, the total burden on the output buffer on the driving card (eg the CPU card) would be 50 IC inputs.

A benefit of using the new high speed CMOS logic families (HC, HCT, ACT etc) in place of the previous bipolar (74, 74LS etc) is that they ease things a little, since a CMOS output can drive much greater numbers of CMOS inputs. However there is another limit, and that is speed: each extra burden on the line adds to the capacitative load and slows the rate of change of signals, and hence limits the maximum frequency of operation of the whole computer system. Thus even if CMOS logic is used it is beneficial to buffer the signals at each circuit board.

2. Shortening back board signal paths. A persistent difficulty in the design of back boards is coping with noise (the unwanted change in a given signal level when others are changing) and propogation delay of signals along the length of the back board. Both of these problems are aggravated by adding long meandering signals on the boards which plug into the bus. The back board in a full system rack is already

longer than we would like; we have to accept this, but adding several inches of extra signal length on each plug in card is to be avoided if at all possible. The use of buffers close to the card edge means that the circuit traces on the board are isolated from the back board.

3. Development. A major feature of Interak, appreciated by many users, is that they can simply throw together their own quick circuits on a breadboard for some experimental purposes. Although even a quick lash up of a circuit should not be excused the proprieties of correct design, in an emergency (for example a student project to meet a deadline, or a demonstration to impress the managing director) the safety margin which is built in by full buffering elsewhere in the system allows the user under pressure to take some chances without causing a disaster. Experienced computer users will be aware of the difficulties with some commercial systems, which are already so finely balanced that they fall over as soon as anything is added to their basic structure, and so are very tedious to work with when developing new hardware additions.

4. Fault finding. Although of course it never happens to the typical highly skilled Interak constructor, there are some unfortunates who make a mess of everything they do: when they plug in a new card and switch on, the whole computer stops working, and it is very difficult to exercise and probe the new card when the most vital tool (the computer itself) is out of service. In such circumstances the buffers can be removed selectively to allow the area and the nature of the fault to be pinned down. For example without buffer chips a shorted data line on a given board will stop the whole computer working; with a buffer which can be unplugged the board can be installed and probed without "crashing" the whole computer.

5. Repair. Although computers and the chips from which they are made are very reliable, the Interak is at special risk from its users, who (and this is not something to be criticised) can never leave things alone, and are always tinkering with sticky fingers throughout the whole machine. If something nasty is done to the computer then the buffers are there to take the strain. For example if two cards are inadvertently set in conflict, one driving 0's onto the bus and the other driving 1's then at the worst they will start to overheat and fail. The cost of replacing a buffer is hardly a pound or two, but compare this with the cost of replacing one of the specialist modern VLSI chips which may be used on a board and which may cost many times this figure. Better to sacrifice the pawns to save the king.

The buffers at each edge connector act like the water tight bulkheads on a ship, dividing the computer into isolated zones. Without buffers the system dissolves into one homogeneous unit and the whole concept of modularity is

compromised.

Sheet 3 RS232 Interface

(To be continued . . .)

Appendix X

Comparison of Pinout Differences
between SIO-Ø, SIO-1, SIO-2, DART

6th October 1987

Pinouts

Pin Number	DART, SIO-Ø	SIO-1	SIO-2
11	RIA(L)/SYNCA(L)	SYNCA(L)	SYNCA(L)
29	RIB(L)/SYNCB(L)	SYNCB(L)	RxDB
28	RxDB	RxDB	RxCB(L)
27	RxTxCB(L)	RxCB(L)	TxCB(L)
26	TXDB	TxCB(L)	TxDB
25	DTRB(L)	TxDB	DTRB(L)

The "(L)" indicates an active low signal, and the use of this suffix is an alternative to the scheme of putting a bar above the signal.

In the asynchronous application of the SIO chip (ie the one which applies to the QS-1 board) the SYNCA(L) and SYNCB(L) pins become general purpose inputs which can be used in the same manner as the RIA(L) and RIB(L) inputs of the DART. Therefore for our purposes the DART and the SIO-Ø devices are interchangable. (In fact we have heard that the DART is a standard SIO chip packaged under another name. The synchronous part of chip in the DART package may or may not be functional)

Omitted Signal Pins

	DART, SIO-Ø	SIO-1	SIO-2
Omitted Signals	RxCB(L) TxCB(L)	DTRB(L)	SYNCB(L)
Restrictions	The above inputs are combined on a single pin, RxTxCB(L)		

Sufficient flexibility by means of movable shorting jumper

links ("JLinks") has been built into the design of the QS-1 board to allow the use of any of the above devices. However the SIO-1 is not normally favoured by us because of the absence of the often used DTRB(L) signal (Data Terminal Ready, Channel B).

The restriction with the DART and SIO-Ø, viz the receive and transmit clocks (RxCB(L) and TxCB(L)) are combined on Channel B, is not serious because those rare applications which require this can still be served by Channel A of any of the devices, since these are always brought out to separate pins. One common use of split baud rates is the (typically British) foolishness of Prestel style communication at 75 baud transmit and 1200 baud receive at one end and vice versa at the other. (Foolish because transmitting and receiving usually takes place along one telephone connection; it needs special ingenuity to make a wire capable of 1200 baud one way but one sixteenth of that rate the other). Because so few contemporary designers of computers have allowed for these split rates, the modern "intelligent" modems are able to make the speed conversion internally and will interface to the computer at 1200 baud transmit and 1200 baud receive.

Equally the restriction with the SIO-2, ie that SYNCB(L) is not available, is a minor one, since this would probably be used in the same way as the equivalent function on the DART, ie as RIB(L) (Ring Indicator Channel B), in modem applications. Again, the advent of intelligence to modems has resulted in their ability to deal in their own prescribed way with any consequences of detecting ringing on the line, and nowadays we rarely need to examine this signal independently of the modem connection.

Our own (personal) view is that the presence of separated RxCB(L) and TxCB(L) pins is of marginally more benefit than the presence of the SYNCB(L) input pin, so we would favour the SIO-2 over the rest if we were stranded on a desert island and could take with us only one type of SIO chip. Many users however will prefer the DART because it has a less formidable data sheet, being specified only for the "asynchronous" applications (ie ours).

In summary:

All 4 devices are perfectly suitable for use on the QS-1. The SIO-1 seems the least useful for general purposes because it is lacking the signal DTRB(L), ie Data Terminal Ready on the B Channel; the other devices (the DART, the SIO-Ø, and the SIO-2) are equally useful to us as the signals they lack are of little or no importance in the usual application of the QS-1.

Setting Up

Linking on the QS-1 Board Pin Assemblies P12,P13 and P46,P47

It would make an already complicated document even more complicated to discuss further the many different modes of operation of the DART and SIO chips. Therefore we propose now simply to present a standard set of links which will suit the general case.

P12 and P13 relate to the SIO chip number "Ø" which is U2, the upper one of the two large chips on this board; P46 and P47 relate to SIO chip number "1", which is U13, the lower one of the two.

Upper Chip (U2):

P12:

Fit no links. These are termination points only for signals which may be connected or which are already connected in track.

P13:

This "customises" the QS-1 to suit the particular chip in use for U2, as follows

DART, SIO-Ø	SIO-1	SIO-2
P13 Link 2-3	P13 Link 2-3	P13 Link 2-3
P13 Link 5-6	P13 Link 5-6	P13 Link 5-6
P13 Link 7-8	P13 Link 7-8	P13 Link 8-9
P13 Link 9-1Ø	P13 Link 9-1Ø	P13 Link 1Ø-11
P13 Link 12-13	P13 Link 11-12	P13 Link 12-13
P13 Link 14-15	P13 Link 13-14	P13 Link 14-15
P13 Link 16-17	P13 Link 15-16	P13 Link 16-17

The links on pins assembly P13 pins 2-3 connect RIAØ(L) to RIA(L)

Upper Chip (U2):

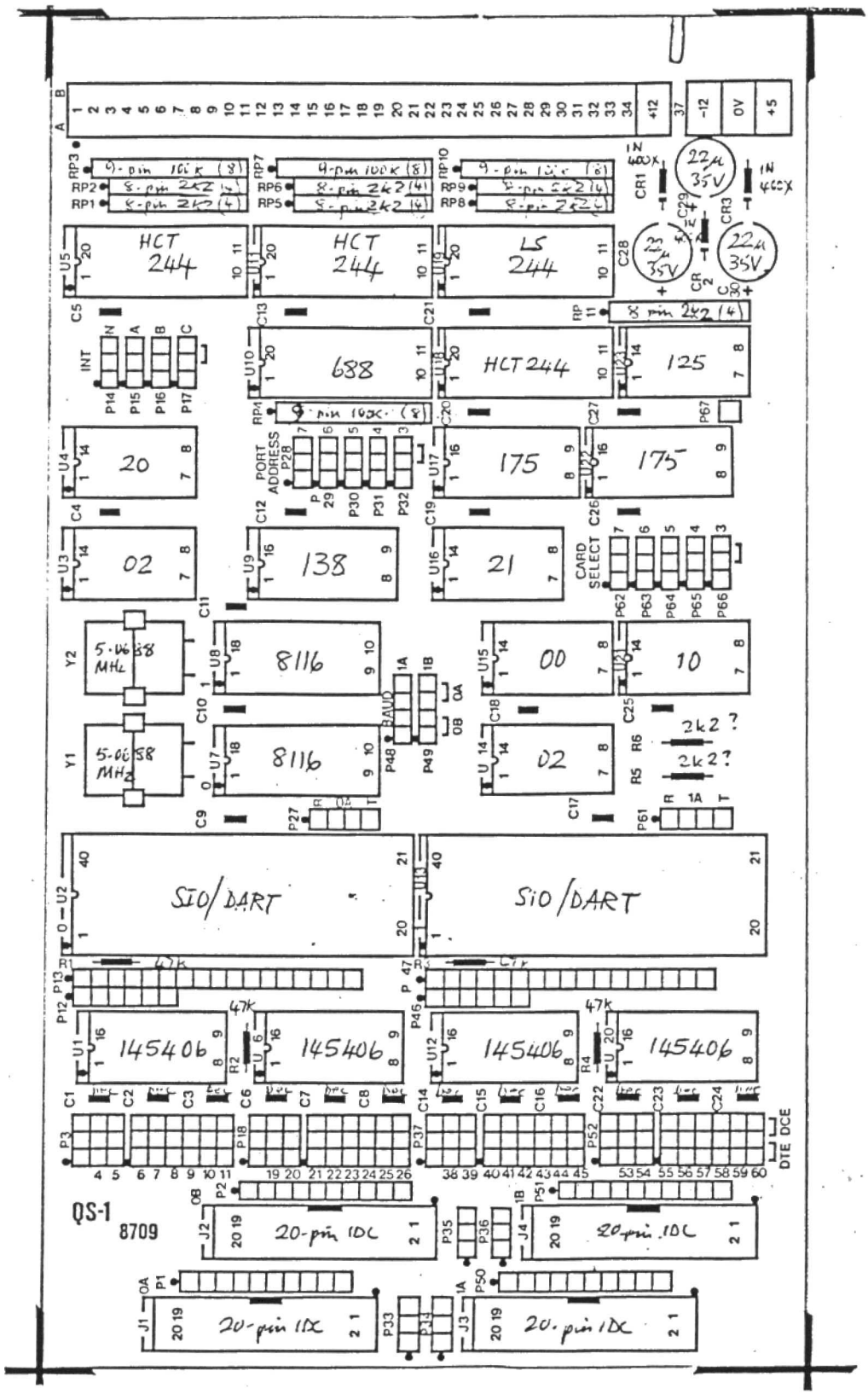
P46:

Fit no links. These are termination points only for signals which may be connected or which are already connected in track.

P47:

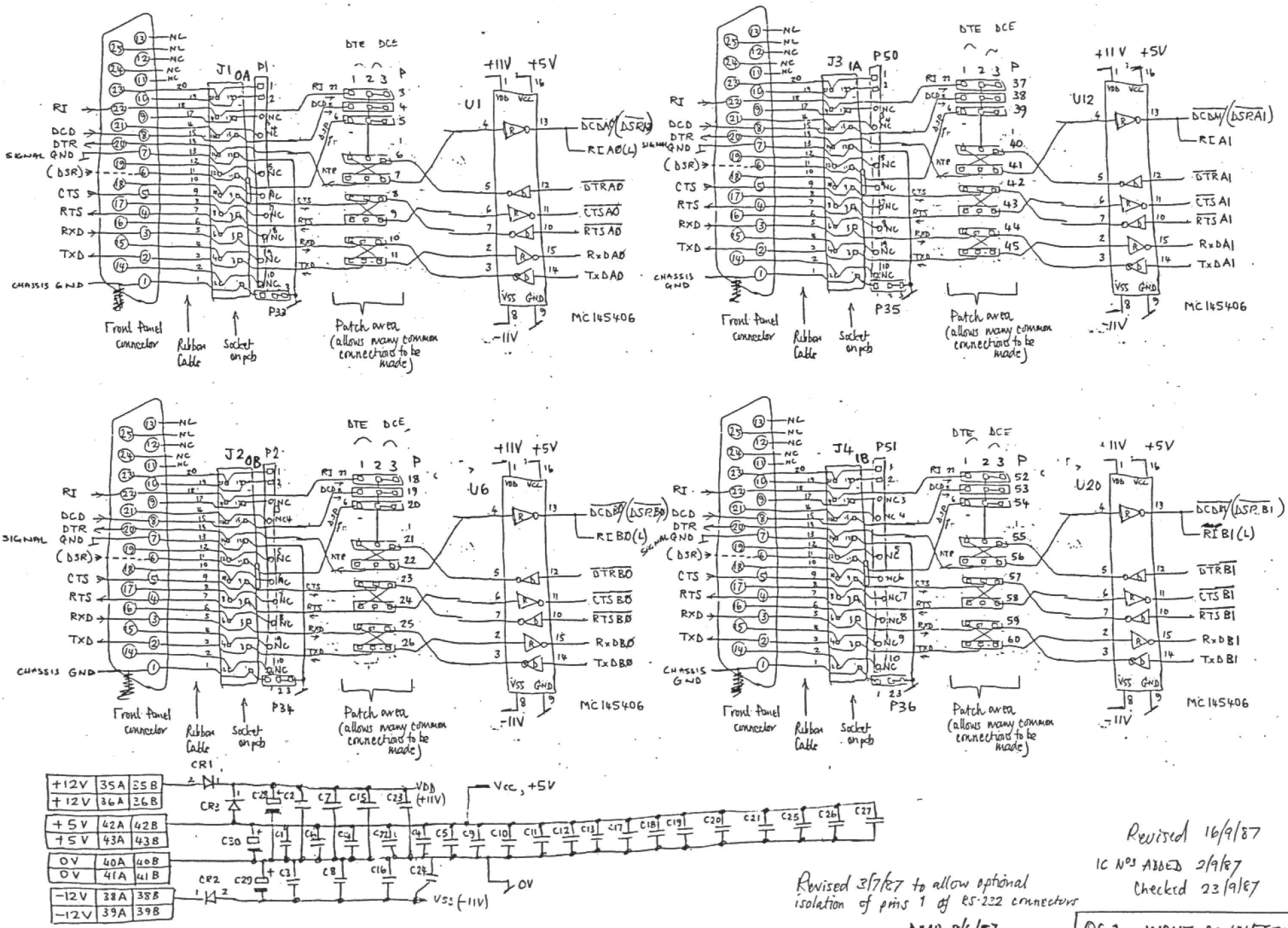
This "customises" the QS-1 to suit the particular chip in use for U2, as follows

DART, SIO-Ø	SIO-1	SIO-2
P47 Link 2-3	P47 Link 2-3	P47 Link 2-3
P47 Link 5-6	P47 Link 5-6	P47 Link 5-6
P47 Link 7-8	P47 Link 7-8	P47 Link 8-9
P47 Link 9-1Ø	P47 Link 9-1Ø	P47 Link 1Ø-11
P47 Link 12-13	P47 Link 11-12	P47 Link 12-13
P47 Link 14-15	P47 Link 13-14	P47 Link 14-15
P47 Link 16-17	P47 Link 15-16	P47 Link 16-17



28 SEP 1987

PROVISIONAL PARTS ALLOCATION

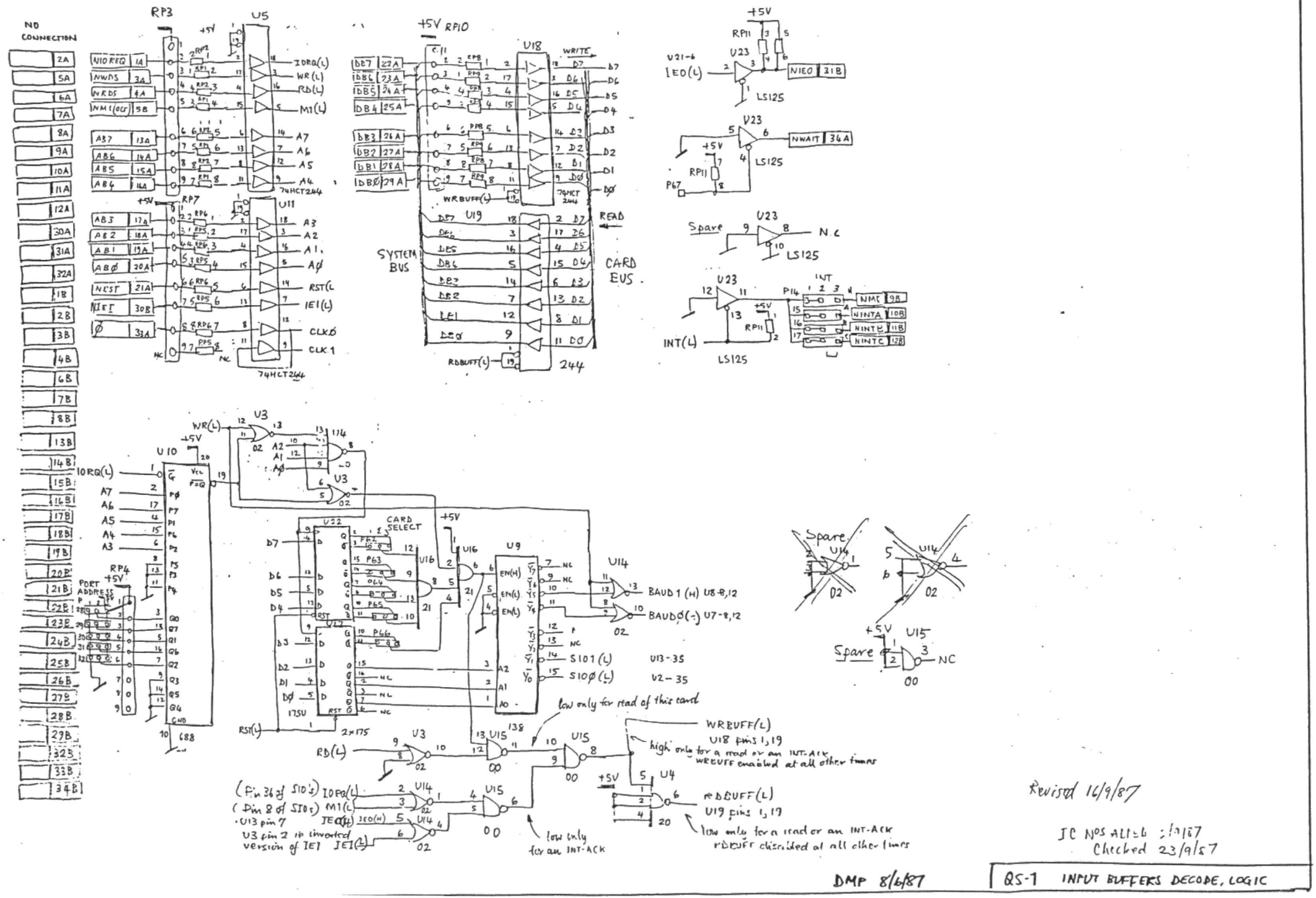


Revised 16/9/87
IC Nos ADDED 2/9/87
Checked 23/9/87

Revised 3/7/87 to allow optional isolation of pins 1 of RS-232 connectors

DMP 8/6/87

QS-1 INPUT CONNECTIONS

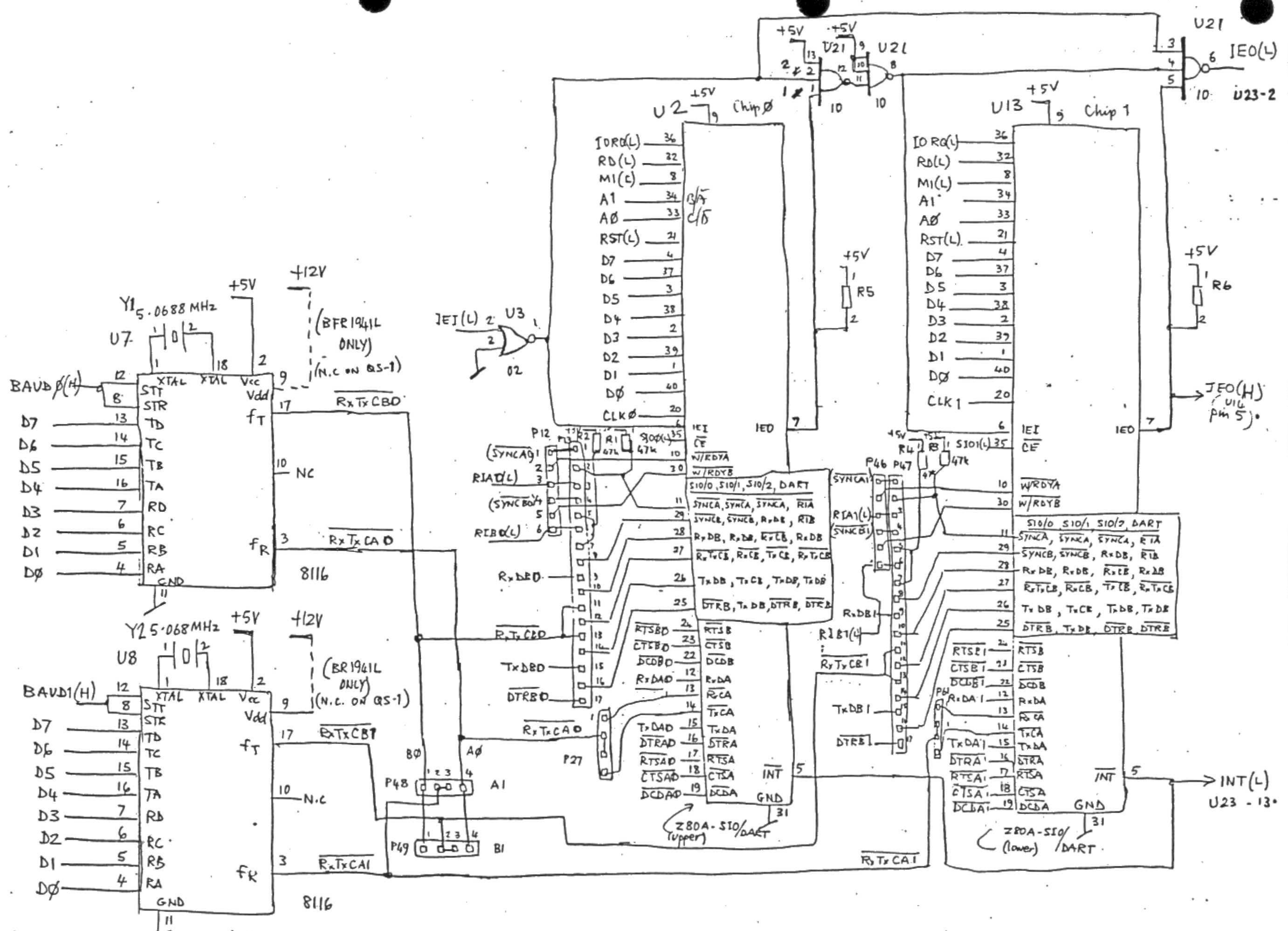


Revised 16/9/87

IC Nos All ± 23/9/87
Checked 23/9/87

DMP 8/6/87

QS-1 INPUT BUFFERS DECODE, LOGIC



Only fitted in those special circumstances where the second SIO dual UART chip must have baud rates different from those used for the first SIO dual.

Revised 16/9/87

IC NOS ADDED 2/9/87

Checked 22/9/87

MOD DMP 8/6/87

DMP 15/5/87 QS-1 BAUD, SIO CHIPS

COMPONENT PRICE LIST FOR QS-1 CARD — List Ref: QS-1/P2
(Prices exclude VAT) — 1 February 88

Resistors (Ø.25W and SIL)

CR2547K	4	R1-4	@ Ø.Ø2	Ø.Ø8	
CR252K2	2	R5-6	@ Ø.Ø2	Ø.Ø4	
SIL Resistors (Use Sockets)					
SIL8-1ØØK	4	RP3,4,7,1Ø (8 x 1ØØk)	@ Ø.26	1.Ø4	
SIL4-2K2	7	RP1,2,5,6,8,9,11 (4 x 2k2)	@ Ø.26	1.82	
	17		RQS1	2.98	2.98

Capacitors
("MAL" = Low Leakage Miniture Aluminium Electrolytic; "CER" = Ceramic; "DEC = 47n-1ØØn Decoupling Grade Polyester, or Ceramic.)

DEC	27	C1-27	@ Ø.Ø9	2.43	
MAL22U	3	C28-3Ø	@ Ø.Ø9	Ø.27	
	3Ø		CQS1	2.7Ø	2.7Ø

Diodes

CR1-3	3	1N4ØØX	@ Ø.Ø6	Ø.18	
	3		DQS1	Ø.18	Ø.18

Quartz Crystals

Y1-2	2	* 5.Ø68ØØ MHz or * 4.915ØØ MHz	@ 1.9Ø	3.8Ø	
	2		YQS1-ØØØ \		
			or	3.8Ø	3.8Ø
			YQS1-5ØØ /		

* use 5.Ø68ØØ MHz with 8116 no suffix
Use 4.915ØØ MHz with 8116-ØØ5

Integrated Circuits
NOTE CMOS Bus Systems: Replace U5, U11, U18 with HC244. Replace U19 with HCT244 if NMOS SIO/DART used, replace U19 with HC244 if CMOS SIO/DART used.

1 x HCØØ	U15	@ Ø.2Ø	Ø.2Ø	
2 x HCØ2	U3,14	@ Ø.2Ø	Ø.4Ø	
1 x HC1Ø	U21	@ Ø.2Ø	Ø.2Ø	
1 x HC2Ø	U4	@ Ø.25	Ø.25	
1 x HC21	U16	@ Ø.25	Ø.25	
1 x HC125	U23	@ Ø.47	Ø.47	
1 x HC138	U9	@ Ø.4Ø	Ø.4Ø	
2 x HC175	U17,22	@ Ø.4Ø	Ø.8Ø	
1 x 74LS244	U19	@ 1.Ø8	1.Ø8	
1 x HC688	U1Ø	@ 1.25	1.25	
2 x 8116	U7,8 (see note above)	@ 5.5Ø	11.ØØ	
4 x 145406	U1,6,12,2Ø	@ 1.89	7.56	
3 x HCT244	U5,11,18	@ Ø.8Ø	2.4Ø	
2 x SIO/DART	U2,13	@ 4.9Ø	9.8Ø	
23		ICQS1-ØØØ\		
		or	36.Ø6	36.Ø6
		ICQS1-ØØ5/		

DIL and SIL Sockets

SCON9	4	RP3,4,7,1Ø	@ Ø.Ø6	Ø.24	
SCON8	7	RP1,2,5,6,8,9,11	@ Ø.Ø6	Ø.42	
DIL14	7	U3,4,14,15,16,21,23	@ Ø.1Ø	Ø.7Ø	
DIL16	7	U1,6,9,12,17,2Ø,22	@ Ø.1Ø	Ø.7Ø	
DIL18	2	U7,8	@ Ø.16	Ø.32	
DIL2Ø	5	U5,1Ø,11,18,19	@ Ø.22	1.1Ø	
DIL4Ø	2	U2,13	@ Ø.3Ø	Ø.6Ø	
34			SKQS1	4.Ø8	4.Ø8

list continues on next page

QS-1 COMPONENT PRICE LIST continued, — List Ref: QS-1/P2
(Prices exclude VAT)

Pin Assemblies

P1-2	2	@ 1Ø pin			
P3-11	9	@ 3 pin			
P12	1	@ 6 pin			
P13	1	@ 17 pin			
P14-26	13	@ 3 pin			
P27	1	@ 4 pin			
P28-45	18	@ 3 pin			
P46	1	@ 6 pin			
P47	1	@ 17 pin			
P48-49	2	@ 4 pin			
P5Ø-51	2	@ 1Ø pin			
P52-6Ø	9	@ 3 pin			
P61	1	@ 4 pin			
P62-66	5	@ 3 pin			
P67	1	@ 1 pin not fitted			
	67				
make from 8 @ 36 pin			@ Ø.89	7.12	
			PNQS1	7.12	7.12

Sundry

63 x J Link			@ Ø.2Ø	12.6Ø	
J1-4	4	2Ø way IDC low prof IDCPSLP2Ø	@ 1.1Ø	4.4Ø	
			SYQS1	17.ØØ	17.ØØ

Total (excluding VAT) Kit Order Code PQS1K4 73.92

OPTIONS (ie Items not included in standard kit of parts)

		(Prices each exclude VAT)
QS-1 Bare Board	BQS1	21.5Ø
1" Card Front Kit, inc fixing and mtg. brackets new type	CF1	2.99
1" Card Front Kit, inc fixing and mtg. brackets original type (RS)	OCF1	4.22
2" Card Front Kit, inc fixing and mtg. brackets new type	CF2	3.92
2" Card Front Kit, inc fixing and mtg. brackets original type (RS)	OCF2	5.36
25 way 'D' Socket (solder bucket) metal	D25S	1.68
25 way 'D' Plug (solder bucket) metal	D25P	Ø.98
25 way 'D' Plastic Hood with screw jacks (do not suit IDC connectors)	D25CP	1.68
IDC 25 way 'D' Socket metal	IDCD25S	3.25
IDC 25 way 'D' Plug metal	IDCD25S	2.98
Pair of female Screwlock assemblies for fastening metal 'D' connectors to front panels	DSL8	Ø.55
Pair of male Screwlock assemblies for retaining cable mounted IDC metal 'D' connectors	DSLM	1.12
2Ø way IDC female connector	IDCF2Ø	1.7Ø
2Ø way IDC grey ribbon cable (per metre)	IDCR2Ø	1.69

Add 5Øp handling charge to each transaction, and 15%

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